a1 In a first embodiment, the present invention provides: a power amplifier for receiving an input signal at an input terminal and producing an output signal at an output terminal, the output signal corresponding to the input signal, the power amplifier having a first power supply circuit comprising: an amplifier coupled to the input terminal for receiving the input signal and coupled to the output terminal for providing the output signal, the amplifier having a power input terminal for receiving a power input signal; a switching regulator coupled to the power input terminal for providing a switching power signal to the amplifier, wherein the switching power signal forms a first part of the power input signal; a linear regulator coupled to the power input terminal, the linear regulator being selectively engageable to provide a linear power signal to the amplifier, wherein the linear power signal forms a second part of the power input signal; an input signal processing circuit coupled to the input terminal for receiving the input signal and for providing a rectified signal indicating the amount of power required by the amplifier; a control circuit coupled to the input signal processing circuit and to the power input terminal for controlling the switching power signal and the linear power signal in response to an error signal corresponding to the rectified signal and the power input signal; a linear regulator control circuit coupled to the input signal processing circuit for receiving the rectified signal and coupled to the linear regulator for controlling the engagement of the linear regulator in response to the rectified signal.

Please amend the paragraph beginning on page 4, line 14 as follows:

a2 In a second embodiment, the present invention provides a power amplifier for receiving an input signal at an input terminal and producing an output signal at an output terminal, the output signal corresponding to the input terminal, the power amplifier having a first power supply circuit comprising: an EMI isolation circuit coupled to the input terminal for receiving the input signal and to an internal input node for providing an EMI-decoupled signal corresponding to the input signal; an amplifier coupled to the input terminal for receiving the input

signal and coupled to the output terminal for providing the output signal, the amplifier having a power input terminal for receiving a power input signal; a switching regulator coupled to the power input terminal for providing a switching power signal to the amplifier, wherein the switching power signal forms a first part of power input signal; a linear regulator coupled to the power input terminal, the linear regulator being selectively engageable to provide a linear power signal to the amplifier, wherein the linear power signal forms a second part of the power input signal; an input signal processing circuit coupled to the internal input node for receiving the EMI-decoupled signal and for providing a rectified signal indicating the amount of power required by the amplifier; a control circuit coupled to the internal input signal processing circuit and to the power input terminal for controlling the switching power signal and the linear power signal in response to an error signal corresponding to the rectified signal and the power input signal; a linear regulator control circuit coupled to the input signal processing circuit for receiving the rectified signal and coupled to the linear regulator for controlling the engagement of the linear regulator in response to the rectified signal.

Please add the following paragraphs beginning on page 5, line 6 as follows:

A3 A power amplifier for receiving a first input signal at a first input terminal and for producing a first output signal at a first output terminal, the first output signal corresponding to the first input signal, a first signal amplifier being coupled to the first input terminal to receive the first input signal and coupled to the first output terminal to provide the first output signal, the first signal amplifier having a first power terminal for receiving a total power signal and the power amplifier having a first power supply circuit comprising: a first input signal compensation block coupled to the first input terminal to receive the first input signal and to provide a compensated input signal corresponding to the first input signal, wherein the compensated input signal defines a target power level; a power signal compensation block for receiving the total power signal and for providing a compensated power signal corresponding to the total power signal; a summer

coupled to the first input signal compensation block and to the power signal compensation block for providing an error signal corresponding to a difference between the target power level and a power level of the total power signal; a control circuit coupled to the summer for receiving the error signal and for providing a first control signal and a second control signal in response to the error signal, wherein the first control signal corresponds to a target main power signal level and the second control signal corresponds to a target transient power signal level; a transient detect block coupled to the first input signal compensation block for providing a transient signal to identify a transient condition when a rate of change in a slew rate of the compensated input signal exceeds a selected transient threshold; a main power supply for providing a main power signal at the first power terminal in response to the first control signal; and a selectively engageable transient power supply for providing a transient power signal at the first power terminal in response to the second control signal and the transient signal, wherein the transient power supply is engaged when the transient signal indicates that a transient condition exists; wherein the control circuit provides the first and second control signals such that the target main power signal level is equal to or higher than the target transient power signal level and wherein the magnitude of the total power signal is generally equal to the higher of the magnitude of the main power signal or the magnitude of the transient power signal.

A power amplifier for receiving a first input signal at a first input terminal and for producing a first output signal at a first output terminal, the first output signal corresponding to the first input signal, a first signal amplifier being coupled to the first input terminal to receive the first input signal and coupled to the first output terminal to provide the first output signal, the first signal amplifier having a first power terminal for receiving a total power signal and the power amplifier having a first power supply circuit comprising: a first input signal compensation block coupled to the first input terminal to receive the first input signal and to provide a compensated input signal corresponding to the first input signal, wherein the compensated input signal defines a target power level; a power

signal compensation block for receiving the total power signal and for providing a compensated power signal corresponding to the total power signal; a summer coupled to the first input signal compensation block and to the power signal compensation block for providing an error signal corresponding to a difference between the target power level and the power level of the total power signal; a transient detect block coupled to the first input signal compensation block for providing a transient signal to identify a transient condition when a rate of change in a slew rate of the compensated input signal exceeds a selected transient threshold; a first transient control circuit coupled to the transient detect block for providing first and second digital transient control signals, wherein the first digital transient control signal indicates the occurrence of a transient condition for a first time period in response to the transient signal and wherein the second digital transient control signal indicates the occurrence of a transient condition for a second time period in response to the transient signal, and wherein the second time period is longer than the first time period; a control circuit coupled to the summer for receiving an amplified error signal for providing a first control signal in response to the amplified error signal; a signal combining block for combining the first control signal and the first transient control signal to provide a main power supply control signal; a selectively engageable second transient control circuit coupled to the first transient control circuit for receiving the second digital transient control signal and for temporarily increasing the magnitude of the error signal, wherein the second transient control circuit is engaged and disengaged in response to the second digital transient control signal, the second transient control circuit including a feedback amplifier coupled between the summer and the control circuit to provide the amplified error signal, the feedback amplifier being operative at all times; and a main power supply for providing a main power signal at the first power terminal in response to the main power supply control signal; wherein the total power signal corresponds to the main power signal.

A method of supplying a total power signal to a signal amplifier, comprising: receiving an input signal; producing a compensated input signal corresponding to the input signal, the compensated input signal defining a target

power level for the total power signal; comparing the compensated input signal to a reduced version of the total power signal to produce an error signal; providing first and second control signals in response to the error signal; providing a main power signal using a switching regulator in response to the first control signal, the main power signal being a first part of the total power signal; comparing a rate of change of the compensated input signal to a selected transient threshold to provide a transient signal, the transient signal identifying a transient condition when the rate of change exceeds the transient threshold, the transient threshold corresponding to a maximum slew rate of the main power signal; and engaging a transient power supply to provide a transient power signal in response to the second control signal, when the transient signal indicates the transient condition, the transient power signal being a second part of the total power signal.

A method of supplying a total power signal to a signal amplifier, comprising: receiving an input signal; producing a compensated input signal corresponding to the input signal, the compensated input signal defining a target power level for the total power signal; comparing the compensated input signal to a reduced version of the total power signal to produce an error signal; providing first and second control signals in response to the error signal; providing a main power signal using a switching regulator in response to the first control signal, the main power signal being a first part of the total power signal; comparing a rate of change of the compensated input signal to a selected transient threshold to provide a transient signal, the transient signal identifying a transient condition when the rate of change exceeds the transient threshold, the transient threshold corresponding to a maximum slew rate of the main power signal; and in response to a transient condition, temporarily engaging the switching regulator with a 100% duty cycle for a first time period and temporarily elevating the error signal for a second time period.

A power amplifier for receiving a first input signal at a first input terminal and for producing a first output signal at a first output terminal, the first output signal corresponding to the first input signal, a first signal amplifier being coupled to the first input terminal to receive the first input signal and coupled to the first

output terminal to provide the first output signal, the first signal amplifier having a first power terminal for receiving a total power signal and said power amplifier having a first power supply circuit comprising: a first input signal compensation block coupled to the first input terminal to receive the first input signal and to provide a compensated input signal corresponding to the first input signal, wherein the compensated input signal defines a target power level; a main power signal compensation block for receiving a main power signal and for providing a compensated main power signal corresponding to the main power signal; a first summer coupled to the first input signal compensation block and to the main power signal compensation block for providing a first error signal corresponding to a difference between the target power level and a power level of the main power signal; a first control circuit coupled to the first summer for receiving the first error signal and for providing a first control signal in response to the first error signal, wherein the first control signal corresponds to a target main power signal level; a total power signal compensation block for receiving the total power signal and for providing a compensated total power signal corresponding to the total power signal; a second summer coupled to the first input signal compensation block and to the total power signal compensation block for providing the second error signal corresponding to a difference between the target power level and a power level of the total power signal; a second control circuit coupled to the second summer for receiving the second error signal and for providing a second control signal in response to the second error signal, wherein the second control signal corresponds to a target transient power signal level; a transient detect block coupled to the first input signal compensation block for providing a transient signal to identify a transient condition when a rate of change in a slew rate of the compensated input signal exceeds a selected transient threshold; a main power supply for providing a main power signal at the first power terminal in response to the first control signal; and a selectively engageable transient power supply for providing a transient power signal at the first power terminal in response to the second control signal and the transient signal, wherein the transient power supply is engaged when the transient signal

indicates that a transient condition exists; wherein the magnitude of the total power signal is generally equal to the higher of the magnitude of the main power signal or the magnitude of the transient power signal.

Please amend the paragraph beginning on page 5, line 9 as follows:

94 Figure 1 is a block diagram of a first embodiment of a power amplifier according to the present invention;

Figure 2 illustrates a second embodiment of a power amplifier according to the present invention;

Figure 3 illustrates a third embodiment of a power amplifier according to the present invention;

Figure 4 illustrates a fourth embodiment of a power amplifier according to the present invention;

Figure 5 illustrates the headroom between a power supply signal of the power amplifier of Figure 4 and a pair of input signals to that power amplifier;

Figure 6 illustrates a fifth embodiment of a power amplifier according to the present invention;

Figure 7 illustrates the relationship between a power signal produced by a switching regulator and a low voltage power supply of the power amplifier of Figure 6;

Figure 8 illustrates a sixth embodiment of a power amplifier according to the present invention;

Figure 9 illustrates a pulse of a power signal produced by a resonant switching regulator of the power amplifier of Figure 8;

Figure 10 illustrates a seventh embodiment of a power amplifier according to the present invention;

Figure 11 illustrates part of the feedback control circuit of the power amplifier of Figure 10;

Figure 12 illustrates another part of the feedback control circuit of the power amplifier of Figure 10;

Figure 13 is a timing diagram illustrating the production of PDM control signal of the power amplifier of Figure 10;

Figure 14 illustrates an eighth embodiment of a power amplifier according to the present invention;

Figure 15 illustrates an input filtration circuit according to the present invention which may be used with a power amplifier;

Figure 16 is a block diagram of a ninth embodiment of a power amplifier according to the present invention;

Figure 17 illustrates a tenth embodiment of a power amplifier according to the present invention; and

Figure 18 is a timing diagram illustrating the operation of the power amplifier of Figure 17.

Please amend the paragraph beginning on page 7, line 5 as follows:

a5 Input compensation block 105 is coupled to input terminal 102 to receive input signal 130 and to provide a compensated input signal 140 at a terminal 117. Amplifier 104 receives a power signal V_t from a positive power terminal 136. Power signal V_t is the sum of a power signal V_s provided by main power supply 118 and a power signal V_l provided by transient power supply 123. The voltage of power signal V_t is equal to the greater of the voltages of power signals V_s and V_l. Output power signal compensation block 135 is coupled to positive power terminal 136 and provides a compensated power signal V_{tr}, which has a range comparable to that of compensated input signal 140. Summer 137 compares compensated input signal 140 to compensated power signal V_{tr} and provides an error signal 139.

Please amend the paragraph beginning on page 8, line 14 as follows:

a6 During this finite time, power amplifier 100 enters a "transient operation" and transient power supply 123 is engaged to provide power signal V_s to

amplifier 104. Transient detection block 119 monitors compensated input power signal 140 at terminal 117 and, when a transient that exceeds a selected threshold occurs in input signal 130, transient detection block 119 enables transient power supply 123. The threshold is selected so that transient power supply 123 will be engaged when main power supply 118 is unlikely to be able to provide power signal V_s with a magnitude approximately equal to V_{targ}. The selection of the threshold will depend on the slew rate of main power supply 118.

Please amend the paragraph beginning on page 13, line 3 as follows:

a7 When the frequency of input signal 230 is relatively low, power signal V_s will follow the waveform of output signal 232, with some headroom. As the slew rate of input signal 230 rises, main power supply 218 may be unable to change the magnitude of power signal V_s sufficiently quickly to follow output signal 232, which will have a correspondingly high slew rate. (Main power supply 218, which is a switching power regulator, has an intentionally limited slew rate, which is discussed below, increasing the possibility that this will occur.) When this occurs, power signal V_s will follow the envelope of output signal 232. However, due to the slow slew rate of main power supply 218 and the high slew rate of the output signal 232, power signal V_s may not have any headroom between it and the envelope of output signal 232. In fact, power signal V_s may be able to follow only the average of the envelope of output signal 232 and may actually be lower than output signal 232 at times, and may therefore be insufficient to power amplifier 204.

Please amend the paragraph beginning on page 13, line 16 as follows:

a8 As mentioned above, frequency compensation block 214 increases the amplitude of frequency compensated signal 238 at higher frequencies. As a result, when higher frequencies are present in input signal 230, rectified signal 240 will be magnified in comparison to input signal 230, and therefore, control circuit 216 will regulate main power supply 218 to a higher target power level

V_{targ}. If the increased amplitude of frequency compensated signal 238 at high frequencies is sufficient, then main power supply 218 may provide a sufficient power signal V_s to power amplifier 204.

Please amend the paragraph beginning on page 14, line 17 as follows:

Q9 Returning to a description of power amplifier 200, main power supply 218 will emit some electro-magnetic radiation, which produces electro-magnetic interference (EMI) in nearby electronic devices. As is well understood, the amount of EMI produced by a switching regulator such as main power supply 218 depends on its switching rate. In order to reduce EMI, the switching rate of switch 246 is reduced by selecting a relatively low frequency for PWM control signal 242. The precise frequency chosen for PWM control signal 242 (which is a fixed frequency signal) will depend on the characteristics of load 234, output signal 232 and energy which must be delivered to properly power amplifier 204, among other criteria. A person skilled in the art will be capable of selecting a suitable frequency to balance these considerations with the need to reduce EMI emissions in a particular implementation of the present invention. Reducing the frequency of PWM control signal 242 and the switching rate of switch 246 has several effects.

Please amend the paragraph beginning on page 16, line 14 as follows:

Q10 Eventually, the magnitude of power signal V_s will rise to V_{targ}. At this point, power signal V_s will be sufficient to separately power amplifier 204. Until this time, it is necessary for switch 224 to keep transient power supply 223 engaged. The period for which switch 224 must remain in this state will depend on the slew rate of main power supply 218 and on the rate of change of input signal 230. The slew rate of main power supply 218 may be calculated (or more likely, the slew rate may be pre-determined based on the maximum EMI that power amplifier 200 is permitted to emit and then main power supply 218 may be designed to have the selected slew rate). Threshold 256 is selected to

correspond to this slew rate, so that main power supply 223 will be kept engaged by switch 224 until power signal V_s is able to rise to V_{targ}.

Please amend the paragraph beginning on page 19, line 12 as follows:

all Amplifier 235 is coupled to terminal 236 to receive power signal V_t and operates as in power amplifier 200 to produce reduced power signal V_{tr}. Summer 237 is coupled to rectifier 215 to receive rectified signal 240 and to amplifier 235 to receive reduced power signal V_{tr} and operates as in power amplifier 200 to produce error signal 239. Control circuit 284 receives control signal 239 and produces an analog control signal 292, which is similar to control signal 244 of power amplifier 200. Switch 224 may couple control signal 292 to the gate of linear regulator 226, when transient power supply 223 is required to supply power signal V_t to amplifier 204, in the same manner as described above in relation to power amplifier 200. Power signals V_t and V_s are diode OR'd through diode 251 to produce power signal V_t.

Please amend the paragraph beginning on page 20, line 14 as follows:

a12 Offset block 311a, frequency compensation block 314a and rectifier 315a, which comprise a first input signal compensation block 305a, are coupled to input terminal 302a in the same manner as offset block 211, frequency compensation block 214 and rectifier 215 are coupled to input terminal 202 of power amplifier 200. Rectifier 315a provides a rectified signal 340a corresponding to input signal 330a at terminal 341a. Similarly, offset block 311b, frequency compensation block 314b and rectifier 315b, which comprise a second input signal compensation block 305b, are coupled to input terminal 302b and rectifier 315b provides a rectified signal 340b corresponding to input signal 330b at terminal 341b. Terminals 341a and 341b are coupled to terminal 341 through diodes 360a and 360b. Rectified signals 340a and 340b are diode-OR'd by diodes 360a and 360b, providing a rectified signal 340 at terminal 341, which corresponds

generally to either the highest magnitude of signals 330a and 330b at any particular time. Offset blocks 311and 311b may be configured to compensate for the diode drops caused by diodes 360a and 360b in rectified signals 340a and 340b.

Please amend the paragraph beginning on page 21, line 4 as follows:

a13 Amplifier 304a is coupled to power input terminal 236 through an overload detect block 362a. Amplifier 304a receives power signal V_t and provides output signal 332a. Similarly amplifier 304b is coupled to power input terminal 236 through an overload detect block 362b and provides output signal 332b. Overload detect blocks 362a and 362b are configured to detect overload conditions in their associated amplifiers 304a and 304b. For example, overload detect blocks 362a and 362b may be configured to detect over-current, over-temperature or other overload conditions. If overload detect block 362a detects such a condition in its associated amplifier 304a, then overload detect block 362a will produce an overload signal 366a, which corresponds to the magnitude of the overload condition detected. Similarly, overload detect block 362b will produce an overload signal 366b if an overload is detected in amplifier 304b. Overload signals 366a and 366b are diode OR'd through diodes 364a and 364b to produce a combined overload signal 366, which is subtracted from rectified signal 340 to produce adjusted rectified signal 370. Adjusted rectified signal 370 is used to control the magnitude of power signal V_t. In this way, overload detect blocks 362a and 362b operate to reduce power signal V_t to protect amplifiers 304a and 304b when an overload occurs.

Please amend the paragraph beginning on page 21, line 21 as follows:

a14 Since input signals 330a and 330b are independent of one another, they may have different magnitudes at any point in time. Accordingly, output signals 332a and 332b will have different amplitudes and amplifiers 304a and 304b will

have different power requirements. Power signal V_t is large enough to power the amplifier 304a or 304b with the largest power requirement at any particular time (assuming that no overload condition exists). As a result, one of the amplifiers will receive more power than it requires and will dissipate the excess power.

Please amend the paragraph beginning on page 21, line 28 as follows:

a15 It has been found that the dissipation of this excess power in one of the amplifiers 304a or 304b does not substantially reduce the average efficiency of power amplifier 300. Reference is made to Figure 5, which shows output signals 332a and 332b and power signal V_t. In the portion of the signals shown, output signal 332b is experiencing a peak at time t_1. Output signal 322a is at a typical or average level. A typical audio signal, such as a movie soundtrack or music, may have a peak-to-average magnitude ratio of 8:1 or higher. At time t_1, output signal 332a may have a current of 2 amps and a magnitude of 5 volts while output signal 332b may have a current of 14 amps and a magnitude of 35 volts. (Output signal 332b has 49 times more power than output signal 332a). Typically, output signal V_t may have an average magnitude of 41 volts (which is selected to account for any ripple in output signal V_t, to power the components of both amplifiers 204a and 204b and to provide reasonable headroom in the amplifier 204a or 204b with the higher power requirements) when amplifiers 304a and 304b are called on to produce these output signals 332a and 332b. Accordingly, output signal 332a has a headroom of 36 volts and will dissipate 72 watts of power (i.e. 36 volts x 2 amps). Output signal 332b has a headroom of 6 volts and will dissipate 84 watts (i.e. 6 volts x 14 amps). Amplifier 304b will therefore actually exhibit a high power loss, even though amplifier 304a has a much larger headroom. As a result, the large headroom created in amplifier 304a due to the peak of output signal 304b does not substantially increase the average power dissipated by power amplifier 300 in comparison to the power dissipated in amplifier 304b at the same time. Furthermore, peaks in a typical musical selection or a movie soundtrack occur relatively infrequently (and often

occur on several channels simultaneously) and since the average level of a typical selection is generally less than 1/8th the level of the peaks in the selection, sharing main power supply 218 and transient power supply 223 between more than one amplifier does not result in a substantial change in the overall efficiency of power amplifier 300.

Please amend the paragraph beginning on page 24, line 20 as follows:

q16 This is accomplished by using low voltage power supply 402 when the magnitude of output signal 232 is relatively small. Low voltage power supply 402 is coupled to positive power supply terminal 236 and provides a fixed voltage DC power signal V_{LV} to amplifier 204 at all times. Power signal V_{LV} is diode-OR'd with power signal V_s and power signal V_l through diodes 404 and 251. In power amplifier 400, at any particular time, power signal V_t delivered to positive power input terminal 236 is equal to the highest of power signals V_l, V_s and V_{LV}.

Please amend the paragraph beginning on page 25, line 16 as follows:

q17 Reference is made to Figure 7, which illustrates an average positive half wave of output signal 232 and power signal V_s, V_{LV} and V_t during the corresponding period. The magnitude V_{LV} of low voltage power supply 402 is selected to be a fraction of the average magnitude $V_{s\text{-}avg}$ of power supply V_s during periods when output signal 232 is at an average level (i.e. a period during which no peaks occur). During such periods, transient power supply 223 will generally not be engaged. During the period shown in Figure 7, transient power supply 223 is disengaged. Between times t_2 and t_3 and between times t_4 and t_5, the magnitude of output signal 232 is less than the magnitude of power signal V_{LV} and power signal V_t is equal to power signal V_{LV}. As noted above, control circuit 216 may be configured to disengage main power supply 418 by setting control signal 442 to 0. In power amplifier 400, control circuit 416 is configured to disengage main power supply 418 when the magnitude of output signal 232 is less than a selected threshold V_d. When the magnitude of output signal 232

approaches threshold V_d, main power supply 418 is engaged by control circuit 416 to produce power signal V_s. Threshold V_d must be selected to ensure that main power supply 418 is engaged whenever power signal V_{LV} would be insufficient to power amplifier 204 to produce output signal 232. In selecting threshold V_d, the desired headroom (defined above as $V_{targ} - V_{req}$) must be taken into account. When main power supply 418 is engaged, power signal V_t will be equal to the higher of power signal V_{LV} and V_s.

Please amend the paragraph beginning on page 27, line 5 as follows:

a18 Positive half circuit 508 is similar to positive half circuit 408 of power amplifier 400, except that control circuit 416 has been replaced with a pulse density modulation (PDM) control circuit 516 and main power supply 418 has been replaced with a main power supply 518 which is a resonant switching power regulator. Main power supply 518 may be any type of resonant switching regulator such as a zero-current-switching (ZCS) converter, a zero-voltage-switching (ZVS) converter, a zero-voltage-switching quasi-resonant converter (ZVS-QRC), a zero-voltage-switching multi-resonant converter (ZVS-MRC), a constant-frequency, a zero-voltage-switching quasi-resonant converter (CF-ZVS-MRC). Such converters are described in U.S. Patent 4,720,668, entitled "Zero Voltage Switching Quasi Resonant Converters" and in U.S. Patent 5,479,337, entitled "Very Low Power Loss Amplifier for Analog Signals Utilizing Constant-Frequency Zero-Voltage Switching Multi-Resonant Converter". Such regulators have the advantage of lower EMI emissions and lower switching losses than the non-resonant main power supplies 218, 318 and 418 described above in respect of power amplifiers 200, 280, 300 and 400.

Please amend the paragraph beginning on page 28, line 7 as follows:

a19 Main power supply 518 receives PDM control signal 542 and produces a power signal $V_{s\text{-}res}$ in response. Power signal $V_{s\text{-}res}$ is analogous to power signal V_s produced by main power supply 218 of power amplifiers 200, 280, 300 and

400. Power signal $V_{s\text{-}res}$ is diode-OR'd with power signal V_I and V_{LV} to produce power signal V_t, which is received by amplifier 204 at terminal 236.

Please amend the paragraph beginning on page 28, line 30 as follows:

a20 The constant on-time of PDM control signal 542 is selected to exceed time period t_8, so that when switch 546 is opened at time t_7 (or later), switch 546 will essentially open a circuit which is carrying no current. During pulse 576, capacitor 574 will have become charged, and when switch 546 is opened, capacitor 574 will have no voltage across it but will have a charge on it. After switch 546 is opened, this charge is discharged into filter 550. The minimum off-time of PDM control signal 542 is selected to allow the charge on capacitor 574 to be essentially completely discharged. If the minimum off-time is too short, a charge will build up on capacitor 574 and the resonant operation of main power supply 518 will be degraded. The structure of PDM control circuit 516 is described below (Figure 11).

Please amend the paragraph beginning on page 29, line 9 as follows:

a21 Reference is again made to Figure 8. As switch 546 opens and closes in response to PDM control signal 542, a series of pulses 576 are generated, forming a power signal $V_{si\text{-}res}$. LC filter 550 smooths power signal $V_{si\text{-}res}$ to produce power signal $V_{s\text{-}res}$. The magnitude of power signal $V_{s\text{-}res}$ during a particular time period will depend on the density of pulses 576 in power signal $V_{si\text{-}res}$. Power signal $V_{s\text{-}res}$ is diode-OR'd with power signal V_I and V_{LV} by diodes 251 and 404 to form power signal V_t, which is provided to power amplifier 204 at terminal 236.

Please amend the paragraph beginning on page 29, line 20 as follows:

a22 Since PDM control signal 542 has a minimum off-time between each pulse 576 (Figure 9), switch 546 cannot have a duty cycle of 100%. As a result, power

signal $V_{s\text{-}res}$ has a lower magnitude than the magnitude $V_{max\text{-}res}$ of power supply 512 (which is analogous to power source 212). To allow power signal $V_{s\text{-}r\ s}$ to have the same magnitude as power signal V_s of the power amplifiers described above, the magnitude $V_{max\text{-}res}$ of power supply 512 must be higher than the magnitude V_{max} of power source 212 (Figure 2).

Please amend the paragraph beginning on page 29, line 27 as follows:

a23 Since each pulse 576 produced by switch 546 will be identical, each pulse 576 will transfer a fixed amount of energy first into capacitor 574 and then into filter 550. The magnitude of power signal $V_{s\text{-}res}$ will depend entirely on the density of pulses 576 (i.e. on the variable off-time between pulses). When a low power signal $V_{s\text{-}res}$ is required, the density of pulses 576 may be quite low and the frequency of the pulses may actually be in the audio band. Also, if the density of pulses is low, a large ripple may be seen in power signal $V_{si\text{-}res}$, and if filter 550 has a desirable low time constant (which allows power signal $V_{s\text{-}res}$ to more closely follow the output signal 232, as described above in relation to power signal V_s of power amplifier 400), power signal $V_{s\text{-}res}$ may also have a corresponding large ripple.

Please amend the paragraph beginning on page 32, line 18 as follows:

a24 As noted above, positive half circuit 608 does not include low voltage power supply 402. In addition to regulating the level of power supply $V_{t\text{-}reg}$ when an overload occurs, post regulator 684 also smooths power signal V_t so that power signal $V_{t\text{-}reg}$ has less ripple than power signal V_t. As noted above in relation to power amplifier 400, one reason for using low voltage power supply 402 to eliminate the use of main power supply 218 (or resonant switching regulator 518) was to reduce the problem of a relatively large ripple on power signal V_t when power signal V_t had a relatively low magnitude. Since this ripple will be reduced by post regulator 684, the need for low voltage power supply 402

is reduced. If desired, low voltage power supply 402 may be incorporated into power amplifier 600 and a person skilled in the art will be capable of doing so.

Please amend the paragraph beginning on page 36, line 19 as follows:

a25 In this way, rectified signal 240, power signal $V_{t\text{-}reg}$ and overload detect signal 366 are used to generate error signal 239 and control signal 244. Switch 224 operates in response to differential signal 254 to selectively couple control signal 244 to the gate of linear regulator 226 (Figures 3 and 10).

Please amend the paragraph beginning on page 37, line 19 as follows:

a26 In an identical fashion, buffer B_2 produces a pulse 734 which remains high for a time t_{10} at terminal 730. Time t_{10} of pulse 734 will depend on the time constant of resistor R_{17} and capacitor C_5. Diode D_4 provides a discharge path for capacitor C_5 when the Q output of buffer B_2 is low. In PDM control circuit 516, the values of resistors R_{16} and R_{17} and capacitors C_4 and C_5 are selected so that the time constant of resistor R_{17} and capacitor C_5 is shorter than the time constant of resistor R_{16} and capacitor C_4. As a result, pulse 734 is shorter than pulse 732 (i.e. time t_{10} is shorter than time t_9).

Please amend the paragraph beginning on page 37, line 27 as follows:

a27 The Q-not output of buffer B_1 is coupled to ground through resistor R_{18} and capacitor C_6. The junction of resistor R_{18} and capacitor C_6 forms node 722, which is coupled to the second input of AND gate G_1. When the Q-not output of buffer B_1 becomes high (at the end of pulse 732), resistor R_{18} and capacitor C_6 acts a delay circuit. After a time t_{11}, capacitor C_6 will be sufficiently charged so that node 722 is a high signal. After this time, AND gate will again provide a high signal to the clock inputs CLK of buffers B_1 and B_2 when error signal 239 is a high signal. This may occur immediately or may occur after some delay.

Please amend the paragraph beginning on page 38, line 4 as follows:

a28 The inputs of AND gate G_2 are coupled to terminals 728 and 730 to receive pulses 732 and 734. The output of AND gate G_2 is coupled to terminal 241 to provide PDM control signal 542. As described earlier, PDM control signal 542 regulates the power signal $V_{s\text{-}res}$ produced by main power supply 518. PDM control consists of a series of pulses which have a constant on-time (during which switch 546 (Figure 10) is closed, a minimum off-time following each pulse during which switch 546 must remain open and a variable off-time between pulses which must exceed the minimum off-time and during which switch 546 remains open.

Please amend the paragraph beginning on page 40, line 12 as follows:

a29 Power supply circuit 708 has two input signal compensation blocks 705a and 705b, which respectively comprise offset blocks 311a and 311b, frequency compensation blocks 314a and 314b and rectifiers 715a and 715b. In order to make power supply circuit 708 operative during positive and negative half waves of input signals 730a and 730b, rectifiers 315a and 315b of power amplifier 300 have been replaced with rectifiers 715a and 715b, which are full wave rectifiers and produce full wave rectified signals 740a and 740b which are diode-OR'd by diodes 360a and 360b to produce a full wave rectified signal 740 at terminal 341.

Please amend the paragraph beginning on page 42, line 13 as follows:

a30 Amplifier circuit 804 comprises an op-amp 820, resistors 822, 824 and 826 and a capacitor 828. The negative input terminal of op-amp 820 is coupled to chassis ground 812 through resistor 822 and to the output of op-amp 820 through resistor 824. The positive input terminal of op-amp 820 is coupled to signal input terminal 802a through resistor 826. Signal input terminal 802a is

coupled to chassis ground 812 through capacitor 828. Resistors 822 and 826 are selected to have a large and equal resistance. Resistor 824 is selected to have a resistance much larger than that of resistor 822, thereby forming amplifier 804 into a non-inverting amplifying amplifier. Typically, resistors 822 and 826 may have a resistance greater than 50 kΩ such as 100 kΩ or more and resistor 824 may have a resistance of 1 MΩ. With these values, amplifier 804 will operate as a multiply-by-10 amplifier. Preferably, amplifier 804 is configured to have an amplification of 2 to 20 times, and more preferably it will have a gain of 3 to 15 times.

Please amend the paragraph beginning on page 43, line 6 as follows:

a31 EMI isolation circuit 800 reduces the coupling of EMI generated within positive half circuit 208 and negative half circuit 210 onto input signal 230 within power amplifier 230 as follows. Within the context of EMI isolation circuit 800, any such EMI may be seen as an EMI signal 835 across resistor 836, which is the only coupling between the floating power amplifier ground 814 and the chassis ground 812. Input signal 230 is received across terminal 802a and 802b. Input signal 230 is amplified by amplifier 804, which provides an amplified input signal 842 across nodes 840a and 840b corresponding to input signal 230. Input signal 230 combined with EMI signal 835 form an EMI contaminated input signal 846 across terminal 844a and 844b. EMI contaminated input signal 846 is reduced by amplifier 806, providing an EMI-decoupled input 831 at terminal 202. This EMI-decoupled input signal 831 is then amplified by power amplifier 200, as described above to produce output signal 232.

Please amend the paragraph beginning on page 43, line 19 as follows:

a32 EMI-decoupled input signal 831 will correspond substantially to input signal 230 with a relatively small degree of contamination from EMI signal 835. This effect may be seen through the following example. If input signal 230 has a

magnitude of 3 volts, EMI signal has a magnitude of -1, amplifier 804 has an amplification of 10 and amplifier 806 has an amplification of 0.1, then amplified input signal 842 will have a magnitude of 30, EMI contaminated input signal 846 will have a magnitude of 29 and EMI-decoupled input signal 831 will have a magnitude 2.9. By amplifying input signal 230 by a selected factor before it is contaminated by EMI signal 835 and then reducing EMI contaminated input signal 846 by the same factor, the effect of EMI signal 835 on input signal 230 is reduced by the selected factor, and consequently, the effect of EMI signal 835 on the operation of power amplifier 200 is reduced. It is not necessary that the amplification factor of amplifier 806 be the reciprocal of the amplification factor of amplifier 806. The amplification factors of amplifiers 804 and 806 may be varied to provide a desired degree of reduction of EMI signal 835 and an appropriate input signal for power amplifier 200.

Please amend the paragraph beginning on page 45, line 3 as follows:

a33 When transient detect block 119 detects a change in input signal 130 that requires power amplifier 900 to enter transient operation, transient control circuit 923a generates a high pulse in transient control signal 904, which is OR'd with control signal 942 to produce a main power supply control signal 906. Main power supply control signal 906 is high when either control signal 142 or first transient control signal 904 is high. Control signal 906 is a PWM signal similar to control signal 242 of power amplifier 200, and can have a duty cycle between 0 and 100%, depending on the value of compensated input signal 140. Main power supply 118 is responsive to main power supply control signal 906 and produces power signal V_s with a magnitude corresponding to main power supply control signal 906. When transient control signal 904 is low, main power supply control signal 906 is identical to control signal 142, and main power supply 118 provides power signal V_s as in power amplifier 100. When transient control signal 904 is high, main power supply control signal 906 will be high (i.e. it will have a duty

cycle of 100%), and main power supply 118 will provide power signal V_s at its highest voltage.

Please amend the paragraph beginning on page 45, line 18 as follows:

a34 When transient detect block 119 detects a change in input signal 130 that requires power amplifier 900 to enter transient operation, transient control circuit 923b also generates a low pulse on transient control signal 908. Transient control circuit 923a receives the low pulse and alters transient control signal 904 to increase the magnitude of error signal 939 in response to it. Control circuit 116 receives the increased error signal 939 and increases the duty cycle of control signal 142 in response. After a selected time, transient control circuit 923a ends the high pulse on transient control signal 904 and main power supply 118 becomes responsive to control signal 142. Main power supply 118 will provide power signal V_s with a voltage level corresponding to the increased duty cycle of control signal 142.

Please amend the paragraph beginning on page 45, line 28 as follows:

a35 Transient control circuit 923b includes a fast attack block 910 and a slow release block 912. Fast attack block 910 operates to quickly increase the magnitude of error signal 939 in response to a low pulse on transient control signal 908. Slow release block 912 operates to slowly reduce the increase in error signal 939, until, after a selected time, transient control circuit 923b has no effect on error signal 939. Power amplifier 900 then returns to normal operation.

Please amend the paragraph beginning on page 47, line 1 as follows:

a36 When transient signal 257 becomes high, power amplifier 1000 enters its transient operation. In response to transient signal 257 becoming high, one-shot circuit 1030 provides a high pulse 1034 on transient control signal 1004, causing

main power supply control signal 1006 to become high. Switch 246 of main power supply 218 remains closed while transient control signal 1004 is high, and main power supply 218 provides power signal V_s at its maximum voltage.

Please amend the paragraph beginning on page 47, line 29 as follows:

a37 Diode 1040 is optional and may be provided to prevent current from flowing from node 1054 to node 1056 when capacitor 1042 is charged. Amplifier 1000 (like amplifiers 100, 200, 280, 300, 400, 500, 600, 700 and 900) uses a closed loop feedback through amplifier 235, summer 237 and control circuit 216 to reduce error signal 239 by keeping voltage V_{1056} approximately equal to the voltage V_{1060} of 1060 (to the extent possible, given the limits of main power supply 218). Amplifier 1052, resistor 1050 and 1046 provide an additional feedback loop, to enhance the control of error signal 239 and to keep voltages V_{1056} and V_{1060} approximately equal. Amplifier 1052, resistor 1050 and 1048 may be optionally provided in any of the amplifiers described above. In normal operation, capacitor 1044 will be discharged.

Please amend the paragraph beginning on page 48, line 8 as follows:

a38 At time t_{12}, transient detect block 219 detects a large transient in the level of input signal 230 and sets transient signal 257 high. In response, one-shot circuit 1030 sets transient control signal 1004 high for a selected time period t_{13} and one-shot circuit 1032 sets transient control signal 1008 low for a selected time period t_{14}. Capacitor 1042 begins to discharge through diode 1038 into one-shot circuit 1032, causing voltage V_{1054} to fall. The low voltage of transient control signal 1008 is selected to sufficiently discharge capacitor 1042 so that the one-shot circuit 1032 begins to draw current from node 1056. For example, the low voltage of transient control signal 1008 may be selected to be ground, so that capacitor 1042 is fully discharged (assuming that the length of the low pulse is sufficiently long).